The readout in parallel of several silicon pixel detectors with a large number of pixels requires the developments of a data acquisition system that can handle the amount of data. The described DAQ system consists of a module that holds the sensor and the readout chips, main acquisition board and PC. The detectors are made of high-resistivity silicon pixel detectors, 1mm thick with 1040 square pads with size of 1mm. The front-end is based on VATAGP7 ASIC by Gamma Medica-Ideas. The chip provides a logic trigger signal and an analog output for each pixel. For the control of the ASICs a FPGA based DAQ board has been designed. The DAQ board (MADDAQ) is equipped with an octal, 12-bit analog-to-digital converter, an FPGA chip from Xilinx and fully featured Ethernet physical layer transceiver will transfer data to PC. The implemented FPGA chip gives the possibility to work in parallel of the four different inputs saving time and reducing the dead time of the acquisition process. The full characterization and performance of the system is presented.